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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,721	08/09/2001	Mark Finn	5298-05200/CD01009	4808

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EXAMINER	
DILDINE JR, R STEPHEN	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,721	FINN, MARK	
	Examiner	Art Unit	
	R. Stephen Dildine	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8,9,11,14,15,18,20 and 21* is/are rejected.

7)☐ Claim(s) *5-7, 10, 12-13, 16-17, 19, 22-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 8-9, 11, 14-15, 18 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by McClure et al. (5,424,988). A comparison of applicant's claims and the reference follows:

Applicant's Claims	McClure
1. A semiconductor memory device	Integrated circuits incorporating memory devices can fail (Column 1, line 11)
comprising testmode circuitry	It is desirable to perform rapid testing to expose defects in a device (column 1, lines 33-34)
adapted to maintain a pair of bitlines coupled to a memory cell within the device	if adjacent bit lines or conductors of a memory device (column 1, lines 39-40)
to the same logic state	are placed in the same logic state (column 1, line 40)
wherein the bitlines are not maintained at the logic state during ordinary operation of the device	Memory cells 302 are connected to separate complimentary bit lines BL and OVERLINE [BL] (column 6, lines 25-27)
2. The semiconductor memory device as recited in claim 1, further comprising a direct current from a voltage source	V1 and V2 of FIG 5 for example where V1=V2 is taught (albeit in the negative) at Column 1, lines 33-47
to each of the pair of bitlines during operation of the testmode circuitry.	404 and 406 of FIG 5 for example
3. The semiconductor memory device as recited in claim 2, further comprising a user-determined voltage from the voltage source.	V1 and V2 of FIG 5 for example "Preferably, first voltage level V_1 is the lowest voltage potential likely to be on the bit line during normal operation, usually 0 volts, ground, virtual ground, or, in some cases, -5 volts." (Column 6, lines 37-42)
4. The semiconductor memory device as recited in claim 2, wherein the direct currents flow for a user-determined time.	Adjacent bit lines are held for a selected time at different (where V1=V2 is taught (albeit in the negative) at Column 1, lines 33-47) voltage levels (column 2, lines 6-7)
8. The semiconductor memory device as recited in claim 1, wherein the testmode circuitry is further adapted to hold the bitlines at the same logic state for a user-determined length of time.	Adjacent bit lines are held for a selected time at different (where V1=V2 is taught (albeit in the negative) at Column 1, lines 33-47) voltage levels (column 2, lines 6-7)
9. A system for testing a semiconductor memory device, said system comprising testmode circuitry adapted to maintain a pair of bitlines coupled to a memory cell within the memory device to the snme logic state, wherein the bitlines are not maintained at the logic state during ordinary operation of the device.	Integrated circuits incorporating memory devices can fail (Column 1, line 11) It is desirable to perform rapid testing to expose defects in a device (column 1, lines 33-34) if adjacent bit lines or conductors of a memory device (column 1, lines 39-40) are placed in the same logic state (column 1, line 40) Memory cells 302 are connected to separate complimentary bit lines BL and OVERLINE [BL] (column 6, lines 25-27)

Applicant's Claims	McClure
11. The system as recited in claim 9, wherein the testmode circuitry is further adapted to maintain the pair of bitlines at the same logic state for a user-determined length of time.	Adjacent bit lines are held for a selected time at different (where V1=V2 is taught (albeit in the negative) at Column 1, lines 33-47) voltage levels (column 2, lines 6-7)
	Integrated circuits incorporating memory devices can fail (Column 1, line 11) It is desirable to perform rapid testing to expose defects in a device (column 1, lines 33-34)
14. A method for testing a semiconductor memory device, said method comprising forcing the memory device into a logic state configuration not occurring during normal operation of the device.	if adjacent bit lines or conductors of a memory device (column 1, lines 39-40) are placed in the same logic state (column 1, line 40) Memory cells 302 are connected to separate complimentary bit lines BL and OVERLINE [BL] (column 6, lines 25-27)
15. The method as recited in claim 14, wherein said forcing comprises maintaining each of a pair of bitlines within the device at the same logic state, wherein the bitlines are complementary during normal operation of the device.	are placed in the same logic state (column 1, line 40) Memory cells 302 are connected to separate complimentary bit lines BL and OVERLINE [BL] (column 6, lines 25-27)
18. The method as recited in claim 15, wherein said forcing comprises flowing a direct current through the memory device from a voltage source to each of the pair of bitlines.	V1 and V2 of FIG 5 for example "Preferably, first voltage level V1 is the lowest voltage potential likely to be on the bit line during normal operation, usually 0 volts, ground, virtual ground, or, in some cases, -5 volts." (Column 6, lines 37-42)
20. The method as recited in claim 14, wherein said forcing comprises holding the logic state configuration not occurring during normal operation of the device for a predetermined time.	Adjacent bit lines are held for a selected time at different (where V1=V2 is taught (albeit in the negative) at Column 1, lines 33-47) voltage levels (column 2, lines 6-7)
21. The method as recited in claim 20, wherein said predetermined time is user-variable.	Adjacent bit lines are held for a selected time (clearly, the user selects the time which means that "said predertimined time is user-variable")

Allowable Subject Matter

Claims 5-7, 10, 12-13, 16-17, 19 and 23-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. Stephen Dildine whose telephone number is 703-305-5524. The examiner can normally be reached on M, Tu, Th, F 5:55 am to 4:25 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

R. Stephen Dildine
Primary Examiner
Art Unit 2133

R. Stephen Dildine